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RESEARCH PAPER

Power Quality Measures of Non-Ideal 3-phase Diode Rectifiers and Smoothing Circuits

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A B S T R A C T:

The study of the rectifier LC smooth circuit to minimize the total harmonic distortion (THD) of three phase of non-ideal diode rectifier has been proposed. The input line current has a non- sinusoidal shape and contains harmonic, which has a negative effect on the input power quality and it makes much stress on the load. According to the International Electrotechnical Commission (IEC61000) standards, variety harmonic limitations are defined to be regulated. In this paper, the cost effective solutions such as changing different parameters including load resistance, DC capacitance and inductance and input AC inductance, on the rectifier performance in terms of V load mean, ripple, diode and Capacitor RMS current, fundamental current and considering relevant harmonics up to 1 kHz and the load side voltage (mean value and ripple) have been investigated to find a best way to reduce ripple voltage stress and harmonics. It has been founded that the best way to obtain high V_{load} mean and fewer ripple is increasing the DC-link Inductance. The major purpose here is to reduce the Total Harmonic Distortion (THD) of the line current under different load conditions (from 61.33% to 26.87%).

KEY WORDS: Three phase rectifier, Total Harmonic Distortion (THD), Ripple, Power quality
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1. INTRODUCTION

In last decades, the request for devices which convert AC-DC signals have been increased rapidly, in particularly demands for using power converters in the field of High Voltage Direct Current (HVDC) and high-power machine drives (Mohan, N. and Undeland, T.M., 2007, Hui et al. 2000). Converters can be used for control frequency and voltage deviation, and decreasing total harmonic distortion (THD) (Mohan, N. and Undeland, T.M., 2007).

The main issues in such low power converter is how to minimizing the THD and ripple while increasing the mean load voltage [Hui et al. 2000 and Singh et al. 2004], therefore in recent years, researchers have focused on improving power quality of the rectifier by reducing total harmonic distortion (THD) throughout changing circuit's parameters as a reliable solution [Krismadinata et al 2009, Ivensky, G. and Ben-Yaakov, S., 2001, and Du et al. 2011]. Recently a huge developments and control techniques have been presented to reduce THD [Ameen, H.F. and Ibrahim, Aula, F.T., 2016, B.S., 2016, Ivensky, G. and Ben-Yaakov, S., 2001, and Du et al. 2011]. In this paper an analysis have been done to minimize the total harmonic distortion (THD) of three phase of non-ideal diode rectifier to an acceptable value by changing different parameters such as, Load

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resistance, DC capacitance, AC side inductance and DC inductance. In addition the output signal of each case will be assessed individually based on that mentioned criteria.

Power simulation programing (PSIM Version 12.0.3.0.564) has been used to design the Circuit diagram of three phase non-ideal rectifier. PSIM software is a powerful computer programing for designing and simulation of all electrical and electronic circuits which helps researchers to be able to analyze results in various scenarios through changing parameters value according to the circuit's requirements [Mehar, H. 2013, Kamiriski et al. 2004]. Authors have investigated Rectifier at full load, Rectifier at reduced load, Increasing DC capacitance, Increasing AC side inductance (Capacitive Smooth Only), Increasing DC inductance, and Increasing AC Inductance, moreover; summary of each case has been explained in the performances of all the cases.

2. Circuit Diagram Of The Rectifier

The circuit diagram of the three phase non-ideal diode rectifier is shown in the fig. (1), the circuit is designed through PSIM Simulation tools.

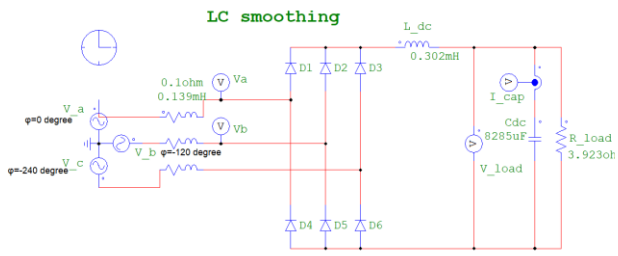

Figure 1: Three phase non-ideal diode rectifier

The above circuit diagram with the input line voltage of 338.4 V while the frequency is 50 Hz contains AC and DC inductances, and DC capacitance, based on that circuit, from the time domain analysis the following parameters have been calculated namely; the load voltage (mean voltage), load ripple voltage, diode peak current, and RMS grid current at the frequency of 300 Hz, while from the Fast Fourier Transform (FFT), the fundamental current up to 19th harmonics will be shown, simultaneously by using that parameters distortion factor and THD can be found, as well as the others. To provide more details and to be concise only three major expressions have been included apart from case A, which full details have been given, therefore; following sections will clarify each case individually.

A- Rectifier at full load

For the circuit as shown in figure (1) with the input voltage (338.4 V, 50 Hz) and output load (R=3.923 ohm, C=8285µF).

From the time domain analysis

1-V load (mean) = $\frac{V\ peak\ (Max)+V\ peak\ (Min)}{2}$

V load mean = $\frac{531.0106+526.207}{2}$ = **528.6088 V**

2-V load (Ripple) =

V peak (Max) − V peak (Min)

V load (Ripple) = 531.0106 − 526.207 = **4.8036 V**

3- Diode Peak Current[A] = **168.929[A]**

4- Cdc (300Hz) RMS Grid Current [A] = **36.704 A.**

From **FFT** Analysis

5- Fundamental RMS Grid Current Line A [Ia] = **105.834 A**

Fundamental peak Grid Current Line A [Ia] = **149.6734A**

nth Harmonic current [%] = [nth Harmonic current (A)/Fundamental current (A)] ∗ 100

3rd Harmonic Current [%] = **0.29360%**

5th Harmonic Current [%] = **30.1041%**

7th Harmonic Current [%] = **9.4677%**

9th Harmonic Current [%] = **0.1346%**

11th Harmonic Current [%] = **7.1077%**

13th Harmonic Current [%] = **4.0085%**

15th Harmonic Current [%] = **0.1213%**

17th Harmonic Current [%] = **3.2888%**

19th Harmonic Current [%] = **2.3962%**

To calculate Total Harmonic Distortion [THD]

$THD=100\sqrt{1-DF^2}$, $DF=\frac{\text{Fundamental RMS current}}{\text{Total RMS Current}}$

Fundamental RMS current input = 149.6734/ $\sqrt{2}$ = **105.8350 A**

Total RMS input current = **111.5095 A**

DF = (105.8350 / 111.5095) = 0.9491

$THD=100\sqrt{1-DF^2} = 100\sqrt{1-0.9491^{\,2}}$ = **31.4974%**

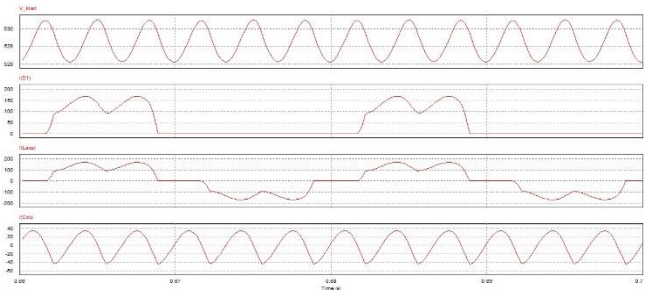

Figure 2: Time domain wave form of (V load, Ia Diode, Ia line, I Cdc) CASE A

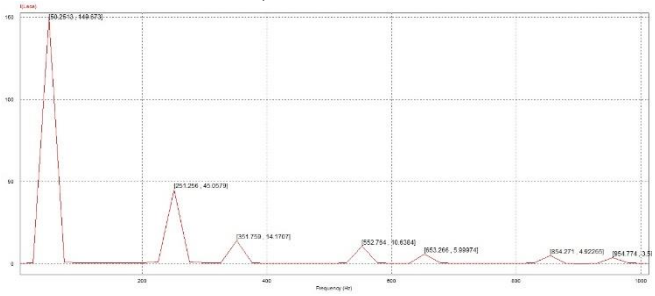

Figure 3: FFT wave form of (Ia line) CASE A

As it can be seen from the fig.2, there is a remarkable ripple, which is calculated around 4.8036 V that makes a problem for the power quality. High ripple means low power quality [Lee et al. 2017]. on another hand, Fig (3) shows that the 5th harmonic value is very high compared with the fundamental harmonic, and then this leads to increase the THD which is 31.4974%. This is due to the fact of having capacitor and inductor in the circuit which are increasing reactive power and it cannot be canceled out [Zobaa, A.F. et al, 2018], therefore we are moving to another case to resolve that problems.

B- Resistance (R) load reduced

When $R\ load\ reduced\ = \frac{R\ load\ at\ full\ load}{5}$, the both ripple voltage and average voltage across the load will change accordingly, due to the short space in this paper, only three significant expression have been presented in this section:

V load (Ripple) = **3.9449 V**

V load (mean) = **555.0998 V**

THD= **61.3364 %**

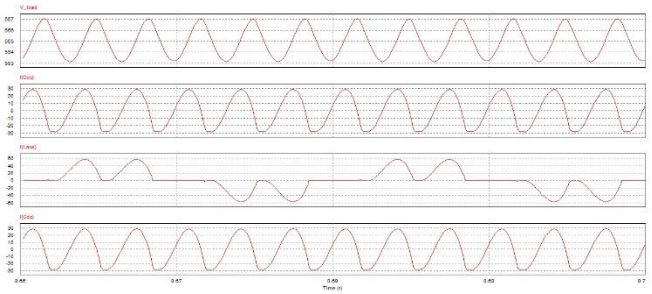

Figure 4: Time domain wave form (V load, Ia Diode, Ia line, I Cdc) CASE B

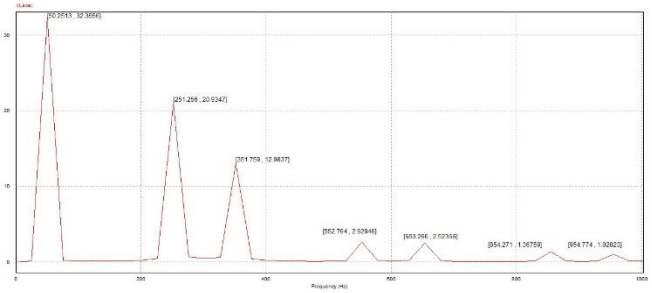

Figure 5: FFT wave form of (Ia line) CASE B

the above figures (fig. 4 and fig.5) shows that, when the load is reduced (increase resistance), the load current reduces as well. Thus, the ripple voltage decreases from 4.8036V at case A to 3.9449V. Similarly, reducing load current is also proportional to the line voltage drop. In another word, ripple voltage of the line decreases and the V load (mean) increases to 555.1V. However, the power quality is appearing to be very bad THD = 61.3364%, which is not desired.

C- Increasing DC-link Capacitance

This time the value of DC capacitance will be four times the values of this capacitance at full load case ($Cdc\ new\ =\ 4\ Cdc\ at\ case\ A$), the parameters will modify as follows:

V load (Ripple) = **1.759 V**

V load (mean) = **528.4983 V**

THD= **31.0724 %**

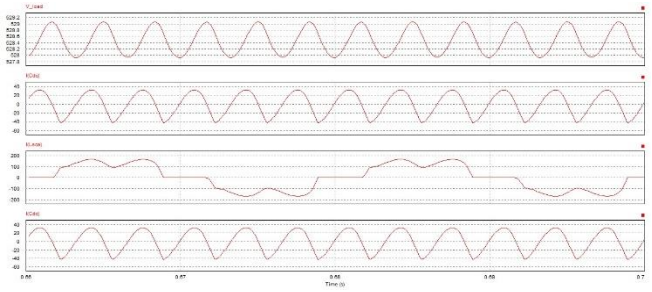

Figure 6: Time domain wave form (V load, Ia

Diode, Ia line, I Cdc) CASE C

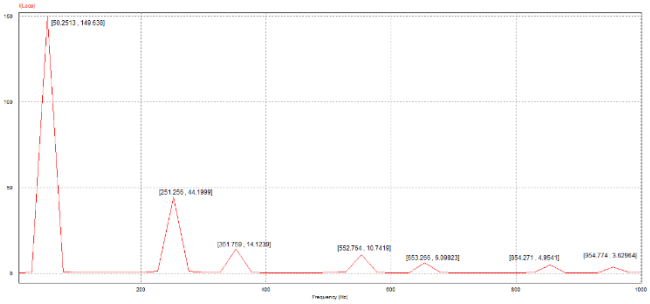

Figure 7: FFT wave form of (Ia line) CASE C

The capacitor always attempts to smooth the output voltage (Mayordomo et al. 2014); it means (fewer ripples). By increasing the capacitance, the ripple reduces from **4.8036V** at case A to **1.759V**, and the capacitor RMS current is also decreasing. The V load (mean) and the diode current is the same as case A, with a better THD=**31.0724 %**

D- ALL Inductance ONLY on AC side

In this occasion, the DC side inductance will be eliminated (Ldc=0), and AC side inductance will be increased by half the ratio of the DC link inductance ($Lac - new = Lac\ at\ case\ A + 0.5 * Ldc\ at\ case\ A$), then the results will appear as below.

V load (Ripple) = **5.579 V**

V load (mean) = **522.6375 V**

THD= **34.9865 %**

It is obvious that most of the ripple voltage is indirectly drops across (Ldc). When Ldc is not connected, the ripple voltage rises to **5.579V.** The diode current is slightly higher than Case A, while capacitor RMS current is still lower. And increasing (Lac) means more line voltage drop. Hence, the V load mean decreases to **522.638V** compared to case A. THD= **34.9865%,** which is higher than case A.

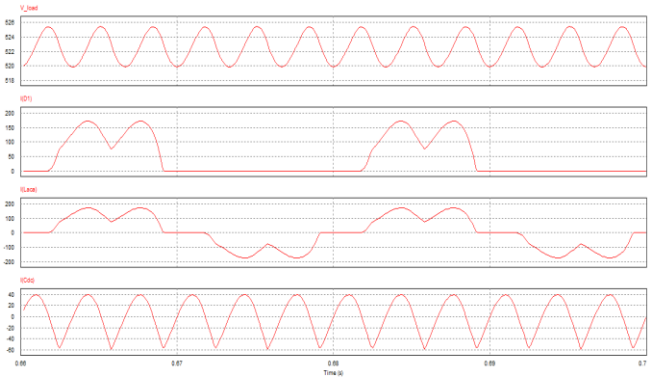

Figure 8: Time domain wave form (V load, Ia Diode, Ia line, I Cdc) CASE D

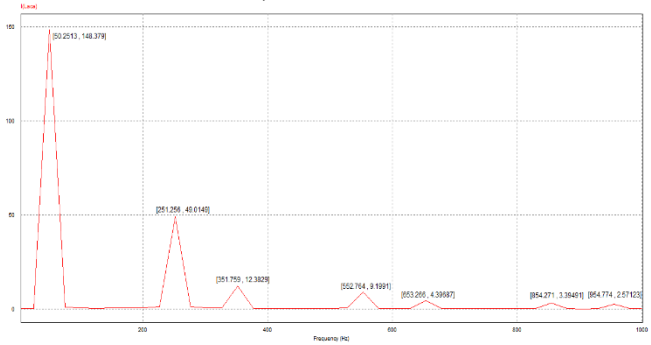

Figure 9: FFT wave form of (Ia line) CASE D

E- Increasing DC-Link Inductance

This case, the new DC side inductance will be three times the DC side inductance (Ldc –new= 3*Ldc at case A), the values for the previous expressions will be as:

V load (Ripple) = **2.2454 V**

V load (mean) = **528.6661 V**

THD= **26.8785 %**

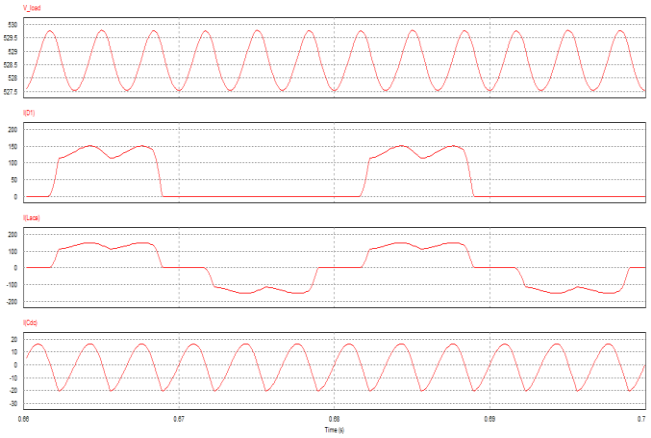

Figure 10: Time domain wave form (V load, Ia Diode, Ia line, I Cdc) CASE E.

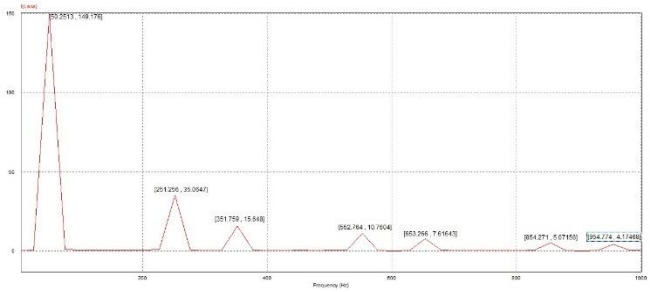

Figure 11: FFT wave form of (Ia line) CASE E.

More ripple voltage drop is obtained by increasing (Ldc), The ripple voltage is reduced to **2.2454 V** which is less than A&D. The diode and capacitor RMS current is less than A&D, and Vload (mean) is the same as A because the Voltage does not drop on Ldc [Prakash et al. 2018, Ertl, H. and Kolar, J.W., 2005]. The power quality is improved and THD=**26.8785%,** which is much better than case A&D.

F- Increasing AC Side Inductance

In the last case AC inductance values will be changed as

(Lac-new= Lac at case A + Ldc at case A), then the three major parameters will change as its shown:

V load (Ripple) = **2.7532 V**

V load (mean) = **517.2288 V**

THD= **26.0773 %**

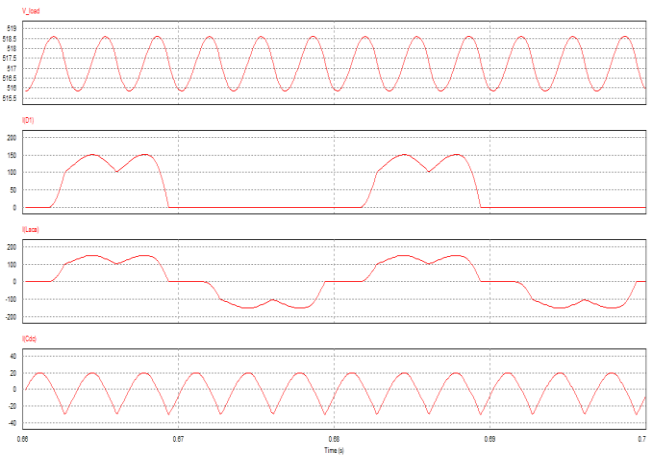

Figure 12: Time domain wave form (V load, Ia Diode, Ia line, I Cdc) CASE F.

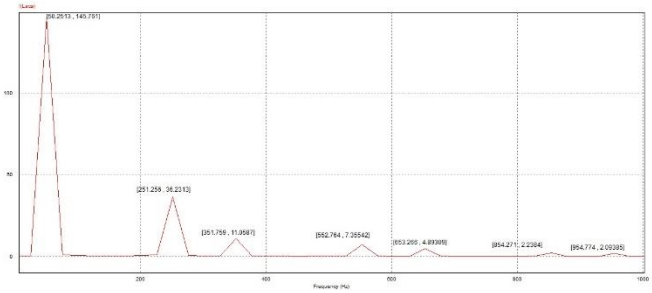

Figure 13: FFT wave form of (Ia line) CASE F.

The higher the value of AC side inductance, leads to the lower the Vload mean=**517.2288 V**, because of the high line voltage drops, and ripple is also lower **2.7532 V** than A, D and greater than E, due to high line inductance. Similarly, the diode current is much lower than A, D and the same as E. Capacitor RMS current is higher than E. THD=**26.0773 %,** which is the lowest value compared to other cases. However, the low Vload mean is not desirable.

3. Performances of analysis

Determining the best case among (A-F) will be based on input power quality and load performance. Results have shown that the voltage does not drop on DC link inductor, and most of the ripple voltage falls on DC Inductor. In another word, high Vload mean and fewer ripples can be obtained by increasing the DC-link Inductance, which is highly preferable by the designers to improve TDH. Therefore, results have proved that increasing the DC-link inductance **(as indicated in CASE E)** is the best way to improve the input power quality, the load voltage and ripple simultaneously. In addition, using DC inductor seems to be cheap economically rather than using AC inductor. Furthermore, the diode current is low and low diode rate for current is required, which is cheaper than high diode current rate.

4. Conclusion

This paper has concerned with reducing THD and Ripple voltage. Several cases have been tested throughout changing circuit's parameters to determine the best way to reduce THD in terms of simplicity and cost effectiveness. Results have shown that V_{load} mean is highly depending on AC side inductance. This means that high AC inductance leads to less V_{load} mean as indicated in Case D&F. According to the obtained results, the ripple voltage also depends on the value of load

resistance, DC inductance, AC inductance, and DC capacitance. High value of (R_{load}, L_{dc}, L_{dc} *and* C_{dc}) less ripple as in case C,E and F. Although the input power quality in Case F is lower than its value in other cases there is much voltage drop due to high AC inductance which is not advantageous. Total Harmonic Distortion (THD) of the line current has been decreased (from 61.33% to 26.87%) under different load conditions. It is highly preferred to replace passive smoothing inductor L by a small power electronic unit such as dc/dc converter.

Acknowledgments

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