ZANCO Journal of Pure and Applied Sciences

TYPE Original Research
DOI http://dx.doi.org/10.21271/ZJPAS.36.3.5

OPEN ACCESS

*CORRESPONDENCE

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RECEIVED 28/09/2023
ACCEPTED 24 /02/ 2024
PUBLISHED 30/06/ 2024

KEY WORDS:

Log amplifier, antilog amplifier, CFTA, Current Mode

A New Current-Mode Log and Antilog Amplifier using Current Follower Transconductance Amplifier (CFTA)

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Abstract:

Log and Antilog Amplifiers are two very important functions in many electronic devices. Thus, in this article a new current mode (CM) log and antilog amplifier using current follower transconductance amplifier (CFTA) are presented. The logarithmic circuit is constructed using only one CFTA as active elements and one metal oxide semiconductor (MOS) transistor as diode operation and antilogarithmic amplifier circuit is implemented using only one CFTA as the active component, one MOS transistor as diode operation and two MOS transistor as active resistors. It provides the advantage of using MOS transistor instead of a resistor and diode that is beneficial to IC implementation in terms of space consideration which are suitable for IC implementation. These circuits provide logarithmic and antilogarithmic responses. Additionally, there is no demand to set selection criteria for components. The operation of the circuit in the current mode was verified by a non-ideality study. PSPICE was used to test the scheme's functioning. The output curves coincide very close with the theoretical expectation.

1. Introduction

Logarithmic and anti-logarithmic amplifiers are nonlinear circuits whose output response is proportional to the logarithmic and exponential value of the input, respectively (Chris et al., 2001, Sanch et al., 2008). They are used for instrumentations, telecommunications, medical equipment's, in the radar and radio receiver, a logarithmic amplifier is employed to compress huge input signal dynamic range active filter and arithmetical operation. Current–mode (CM) circuits provide many advantages including bigger dynamic range, intrinsically wide bandwidth, simpler design, higher linearity, and lesser power consumption. Over the past few decades, op amps have been an essential building block in analog circuit design. Unfortunately, at large closed-loop gains, the constant gain-bandwidth product restricts performance such as bandwidth, slew rate, and restricted bandwidth. Furthermore, op amps have a slew rate restriction, which limits large-signal and high-frequency operation. Analog circuit designers explored for various solutions and building blocks to overcome the disadvantages of op amps and produce high speed systems. These results in the creation of a new active building block with the CM. Due to their broad dynamic range and bandwidth, current-differential buffer amplifiers (CDBA), current-follower transconductance amplifiers (CFTA), current differencing transconductance amplifier (CDTA) have received attention (Surasak et al., 2019 and Başak et al.,2022).

Over the past twenty years, the demand for transportable, rechargeable, low-voltage devices has expanded. Therefore, research has interested on lowering the power supply voltage of analog devices. CM technology is suitable for this purpose as it requires a low-voltage operating circuit (Tangsrirat et al., 2007). Logarithmic circuits require high input dynamic range to compress large-amplitude signals at the radar receiver input, high accuracy of arithmetic functions, and low power consumption (Indu, 2013). A literature review reveals numerous papers dealing with logarithmic and anti-logarithmic amplifiers using the CDTA family of current conveyors and floating current conveyors in OFCC operation. A closer look at the composition reveals that the circuits presented in (Indu et al., 2013, Neeta et al., 2014, Mohammad et al., 2012, and Pandey et al., 2018) are affected by one or more of the succeeding flaws:

1- Overuse of passive parts, particularly resistors as in (Neeta et al., 2014, and Mohammad et al.,2012).
2- Using more than one type of element (Indu et al., 2013, Mohammad et al.,2012, Neeta et al., 2014).
3- Employing the voltage-mode, this circuit has greater power requirements, poor linearity, smaller dynamic range, and less bandwidth. As in (Pandey et al., 2018).
4- Proposed only logarithmic function (Neeta et al., 2014)

In this work, A New Current-Mode Log and Antilog Amplifier using CFTA, the logarithmic circuit is constructed using only one CFTA as active elements and one metal oxide semiconductor (MOS) transistor as diode operation and antilogarithmic amplifier circuit is constructed using only one CFTA as active elements, one MOS transistor as diode operation and two MOS transistor as active resistors. It offers the benefit of using MOS transistor instead of a resistor and diode, it is advantageous for IC implementation, because less space is needed. A summary of characteristics of several Log and Antilog Amplifier function realizations of which reported in (Neeta et al., 2014, Mohammad et al.,2012, Indu et al., 2013, and Pandey et al., 2018) and compare with the proposed circuit are given in Table 1.

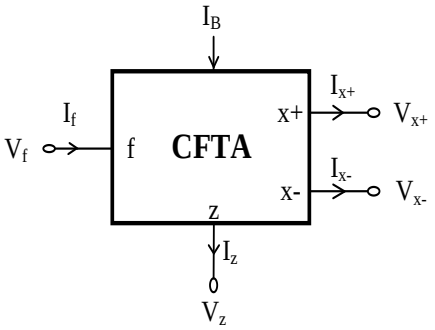
Table 1: Comparative study of the available Log and Antilog Amplifier

Paper	Active element used	Using more than one type of element	Passive elements required	Employing the current-mode
(Mohammad et al. , 2012)	CDTA	yes	yes	yes
(Indu et al., 2013)	CDTA	yes	NIL	yes
(Neeta et al., 2014)	OFCC	yes	yes	yes
(Pandey et al., 2018)	OTRA	NIL	NIL	NIL
(Proposed circuit)	CFTA	NIL	NIL	YES

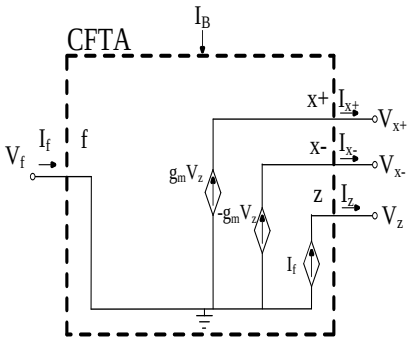
2. Methodology

2.1. CFTA

The CFTA (Nisha et al., 2015), its electrical symbol and electrical equivalent circuit are shown in the Figure 1. Its ideal terminal characteristics are given by the matrix below.



(a)



(b)

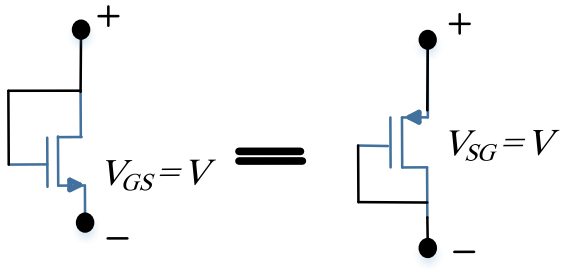
Figure 1: CFTA (a) Symbol (b) Equivalent Circuit

The current follower input stage of the CFTA creates a low impedance at input terminal F. A high impedance intermediate Z-terminal receives a current provided at the input terminal. The Z terminal is typically linked to a grounded impedance in applications. The dropped voltage (V_Z) across the grounded impedance is then changed to current Ix+ and/or Ix- by the transconductance stage. The transconductance (g_m) of the transconductance stage can be externally adjusted by bias current (I_B). The terminal relations are given in the following matrix.

$$\begin{bmatrix} V_f \\ I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & +g_m & 0 & 0 \\ 0 & -g_m & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_f \\ V_z \\ V_{x+} \\ V_{x-} \end{bmatrix}$$

2.2. MOSFET as Diode connection

The MOSFET behaves like a diode with properties of a pn-junction diode when its gate is coupled to its drain, (Chen et al.,2007), as shown in Figure 2.



(a) **(b)**

Figure 2: MOSFET as Diode connection (a) N-MOSFET (b) P-MOSFET

An enhancement MOSFET is always in the saturation area when the gate is linked to the drain.

$V_{DS} \geq V_{GS} - V_T$ (2.1)

$V_D - V_S \geq V_G - V_S - V_T$ (2.2)

$V_D - V_G \geq - V_T$ (2.3)

$V_{DG} \geq - V_T$ (2.4)

Because V_T is always larger than zero for an enhancement device then $V_{GD} = 0$ satisfies saturation condition.

$I_D = ((K'W)/2L)[(V_{GS} - V_T)^2]$ (2.5)

$V_{GS}=V_{DS}=V_T+\sqrt{(2\ I_D/\beta)}$ (2.6)

where $K' = \mu C_{ox}$, μ is carrier mobility, C_{ox} is the gate capacitance per unit area, V_T is the threshold voltage, β is beta $\beta = {}^{K'W}/_{L}$ and L and W are the channel length and width, respectively,

2.3. MOSFET as resistor

By operating the MOSFET in the triode region (Rout et al., 2020) is shown in Figure 3 we have a resistor with a value that can be controlled electronically. These resistors in turn may be used as the control element in more complicated electronic circuits. An important aspect of the utility of the MOSFET in this application comes from the fact that the control signal is well isolated from the resistor terminals.

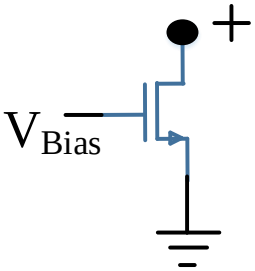


Figure 3: N-MOSFET

$r_{ds}=L_M / (K' W_M (V_{GS}-V_T))$ (2.7)

Where r_{ds} is resistor, $K' = \mu C_{ox}$, μ is carrier mobility, C_{ox} is the gate capacitance per unit area, V_T is the threshold voltage and L and W are the channel length and width, respectively.

2.4. Proposed circuit and its operation

the Proposed current mode CFTA-based Log and antilog amplifier circuit which is shown in Figure 4.

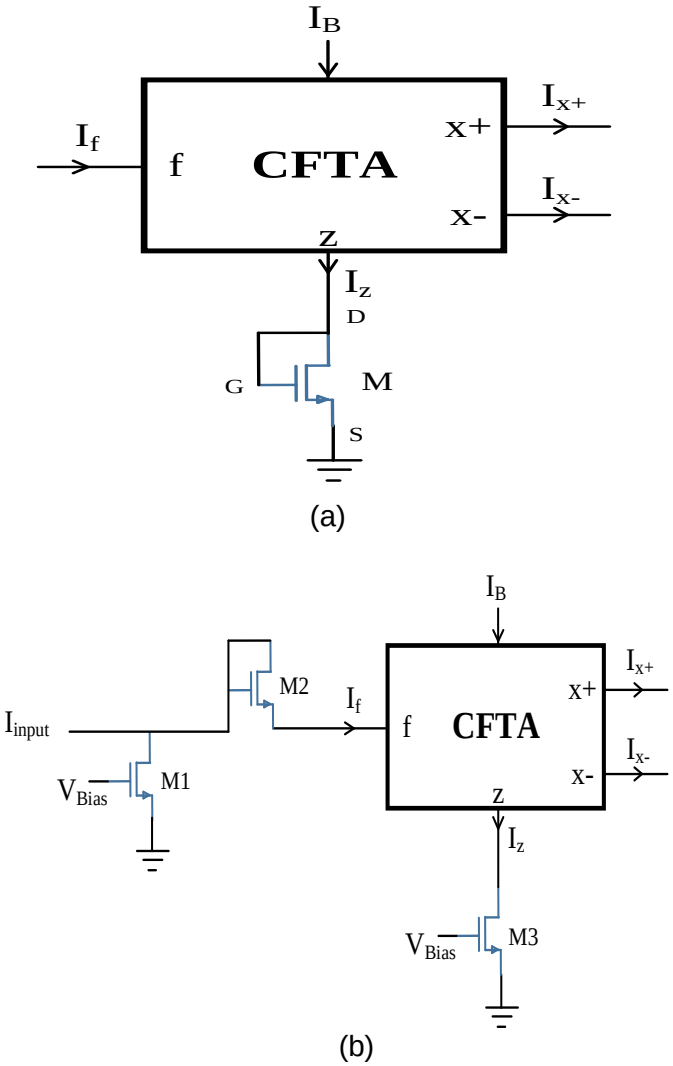


Figure 4: (a) log amplifier realization using CFTA, (b) antilog amplifier realization using CFTA.

Log amplifier In the CM, it is constructed by one CFTA and MOSFET transistor as diode operation as in Figure 4a and antilog amplifier In the CM, it is implemented by one CFTA, MOSFET transistor as diode operation and two MOSFET transistor acts as resistor as in Figure 4b.

In the proposed circuit in Figure 4a and 4b the subscripts $V_Z, V_Z, I_{X+}, \text{and } I_{X-}$ signify the output currents and voltages of Z and X nodes of the CFTA blocks in Figure 4a and 4b.

The proposed circuit analysis of Figure 4a the output current given in Equation (2.8) is obtained

$I_{out} = I_X = g_m V_Z$ (2.8)

where $V_Z=V_{GS}=V_{DS}=V_T+\sqrt{(2\ I_D/\beta)}$

where V_{GS} is the voltage between gate and source and V_{DS} is the voltage between darin and source of transistor M is connected at z-terminal of CFTA, V_T is the threshold voltage, β is beta $\beta = {K'W}/{L}$ and L and W are the channel length and width, respectively, $K' = \mu C_{ox}$, μ is carrier mobility and C_{ox} is the gate capacitance per unit area.

The proposed circuit analysis of Figure 4b the output current given in Equation (2.13) is obtained

$r_{ds1}=L_{M1} / (K' W_{M1}(V_{GS}-V_T))$, (2.9)

$r_{ds3}=L_{M3} / (K' W_{M3}(V_{GS}-V_T))$ (2.10)

Where

r_{ds3} is drain and source resistor

$K' = \mu C_{ox}$, μ is carrier mobility, C_{ox} is the gate capacitance per unit area

V_T is the threshold voltage and L and W are the channel length and width, respectively of the transistor M1 and M3.

$I_{DM2}=\beta/2((V_{GS}-V_T)^2)$ (2.11)

Where I_{DM2} is the drain current, V_T is the threshold voltage, β is beta $\beta = {K'W}/{L}$ and L and W are the channel length and width, respectively, $K' = \mu C_{ox}$, μ is carrier mobility, C_{ox} is the gate capacitance per unit area of the transistor M2.

$I_{out} = I_{X+} = g_m V_Z$ (2.12)

where $V_Z = V_{DM3}$

$I_{out} = I_{X+} = g_m V_{DM3}$ (2.13)

where V_{DM3} is the drain voltage of the transistor M3.

2.5 Non-idealities effects

By considering the non-idealities characteristics of the CFTA, the kinship of the voltages and currents can be rephrased as:

$$\begin{bmatrix} V_f \\ I_z \\ I_{x+} \\ I_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha i & 0 & 0 & 0 \\ 0 & +\beta igm & 0 & 0 \\ 0 & -\beta igm & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_f \\ V_f \\ V_{x+} \\ V_{x-} \end{bmatrix}$$

Where $\propto_i = 1 - \varepsilon_i$ and ε_i ($|\varepsilon_i| \ll 1$) indicate the current gain and $\beta_v = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| \ll 1$) indicate the voltage gain. Reexamination of the proposed circuit yields the modified functions of the presented log and antilog amplifier.

$I_{out} = I_X = \beta_i g_m V_z$ (2.14)

Where $V_Z=V_{GS}=V_{DS}=V_T+\sqrt{(2\, I_D/\beta)}$

The proposed circuit analysis of Figure 4b the output current given in Equation (2.19) is obtained

$r_{ds1}=L_{M1} / (K' W_{M1}(V_{GS}-V_T))$ (2.15)

$r_{ds3}=L_{M3} / (K' W_{M3}(V_{GS}-V_T))$ (2.16)

$I_{DM2}= \beta/2((V_{GS}-V_T)^2)$ (2.17)

$I_{out} = I_X = \beta_i g_m V_z$ (2.18)

where $V_Z = V_{DM3}$

$I_{out} = I_{X+} = \beta_i g_m V_{DM3}$ (2.19)

3. Results and Discussions

The proposed log and antilog amplifier circuits are simulated at room temperature (25°C) by using PSPICE program to validate the theoretical analysis presented. The CFTAs are simulated using the schematic diagram in Figure 5 (Daibor B. et al., 2008, Nisha et al., 2015). The dc supply voltages were selected as $V_{DD} = -V_{SS} = 1.5V$, $V_{BB} = -0.55V$, bias current of the CFTA is $I_B = 100\mu A$ based on 0.25 μm TSMC Complementary Metal Oxide Semiconductor (CMOS) technology the main advantage of this technology is the power dissipation and external Transistor M of the proposed circuit in Figure 4a with the width $W = 20\mu m$ and length of L=1μm is used in the simulation program. External Transistor M1 and M3 of the proposed circuit in Figure 4d with the width $W = 3\mu m$ and length of L=1μm with $V_{BIAS} = 1.5v$ and External Transistor M2 of the proposed circuit in figure 4b with the width $W = 20\mu m$ and length of L=1μm are used in the simulation program. To show the effect of temperature on the proposed circuit Reanalysis the proposed circuit at 30 °C. The output responses of the Log and antilogies confirm the theoretical presupposition. The output responses of the log amplifier are shown in Figure 6 and Figure 7. The output responses of the antilog amplifier are shown in Figure 8 and Figure 9.

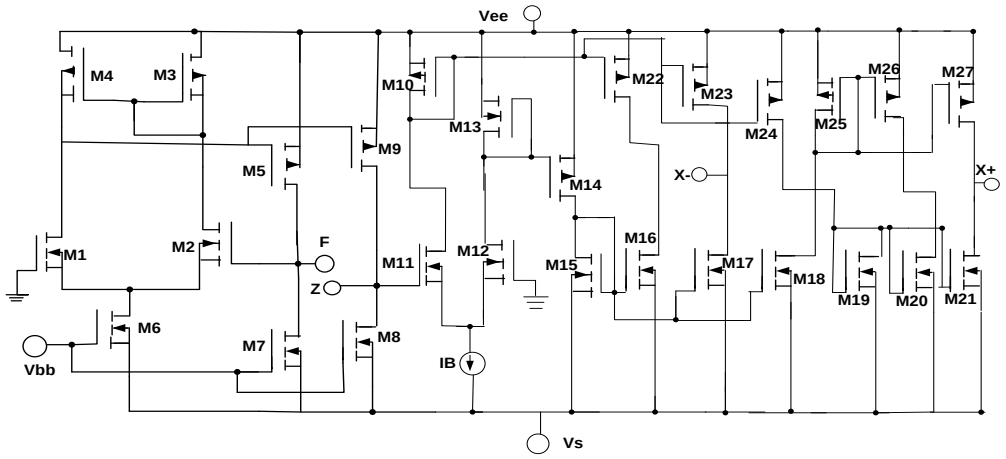


Figure 5: A CMOS schematic structure for CFTA

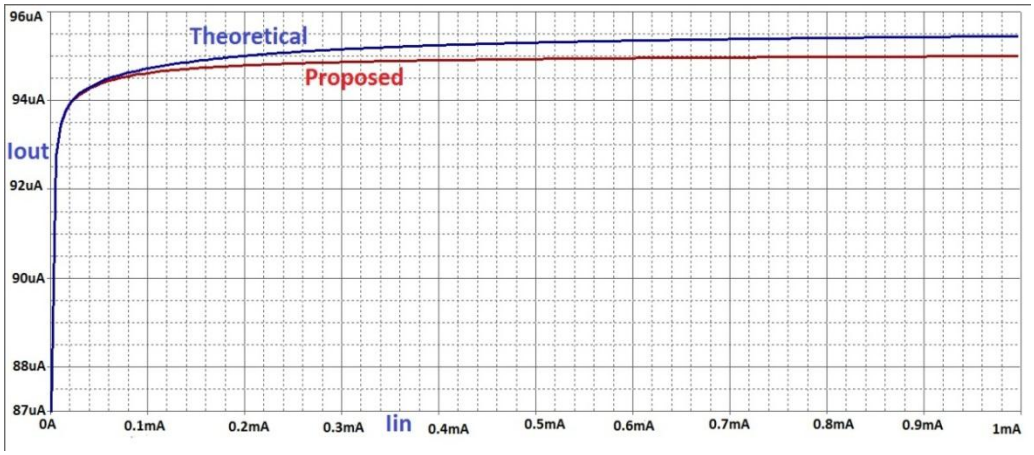


Figure 6: Logarithmic amplifier output at room temperature

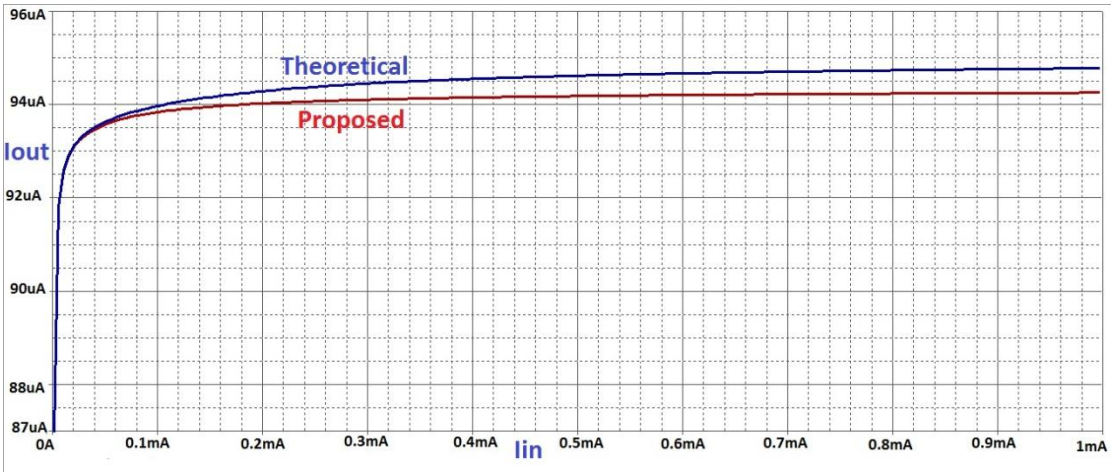


Figure 7: Logarithmic amplifier output at 30 °C temperature

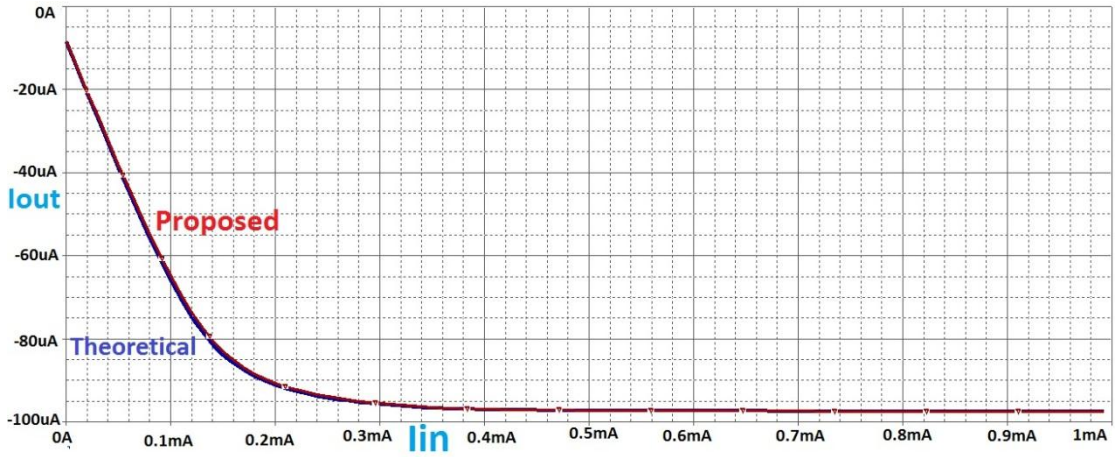


Figure 8: Antilogarithmic amplifier output at room temperature

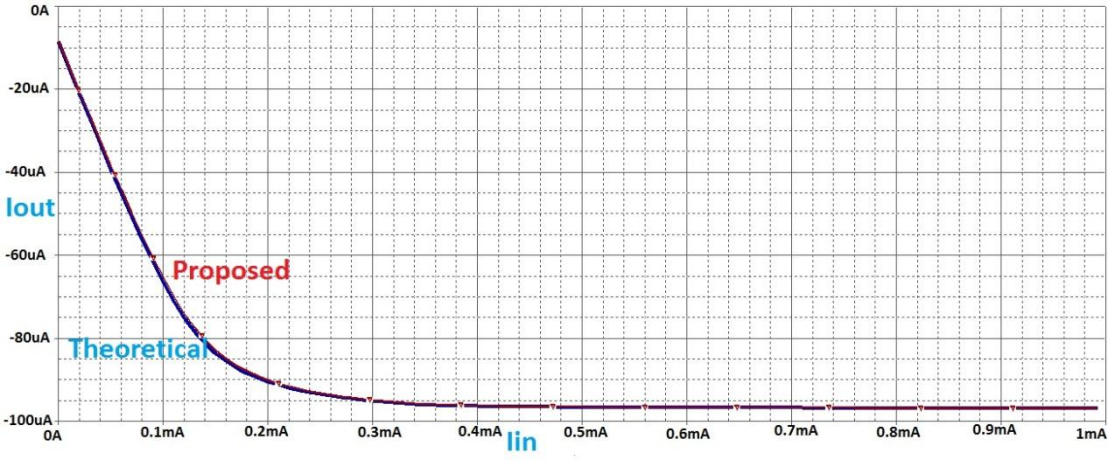


Figure 9: Antilogarithmic amplifier output at 30 °C temperature

From the simulation result of the Logarithmic amplifier in Figure 6 it is found that the output current is proportional to the logarithmic function of the input current and similarly from the simulation result of the Antilogarithmic amplifier in Figure 8 it is found that the output current is

exponentially related to the applied input current and from Figure 7 and 9 it's clear that output current has a inversely relationship with the temperature because temperature has an effect on the threshold voltage of a CMOS device also its it is clear that the simulation results are coincide well with the theoretical evaluations. And the total power dissipation by the proposed circuits are 2.6mW and 2.65mW for Logarithmic and Antilogarithmic amplifiers, respectively. It's clear that the low power dissipate due to current mode operation and using CMOS technology.

4. Conclusions

In this paper a proposed log and antilog amplifier configuration based on current follower transconductance amplifier (CFTA) components has been presented. The proposed logarithmic and Antilogarithmic amplifier circuits have a low input impedance at F-terminal and high output impedance at x- terminal Therefore; these characteristics make the proposed circuit attractive for current mode operation. The pros of the offered log and antilog amplifier configuration are (i) It offers the benefit of using MOS transistor instead of a resistor and diode, that saves space in IC implementation. (ii) The circuit only utilizes active components which is an attractive option for integrated circuit realization (iii) lower supply voltage, less consumption power and a wider frequency band, thanks to operation in current mode. (iv)

Conditions for component selection don't need to be set. The PSPICE simulation results show that the output current of the logarithmic amplifier is a logarithmic function of the input current. The simulation findings of the Antilogarithmic amplifier show that the output current is an antilogarithmic function of the input current, and it is obvious that the simulation results correspond well to the theoretical assessments.

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